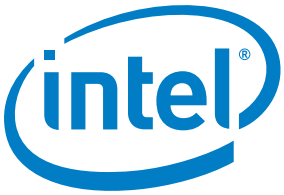

Microsoft* Windows* 7 (WIN7, WES7 & POSReady 7) 32 & 64-bit IO Drivers for Intel® Atom™ Processor x5-E8000 and Intel® Pentium®/Celeron® Processor N3000 Family

Release Notes

March 2016

Intel Confidential

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Revision History

Date	Revision	Description
March 2016	1.2	Maintenance Release 1.
September 2015	1.1	Section 2.3 Updated Best Known Configurations information. Section 2.4 Added eMMC and SD2 driver information. Updated graphics driver naming convention.
July 2015	1.0	Initial release.

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1.0 Introduction

1.1 Scope of Document

This document consists of Release Notes about the Intel developed GPIO*, I²C*, HS-UART and SD/eMMC* driver for Windows* 7, Windows Embedded Standard* 7 and Windows Embedded POSReady 7. This document also includes information about Window* 7 inbox drivers that have been validated on the Intel® Atom™ processor x5-E8000, Intel® Pentium® Processor N3700 and Intel® Celeron® Processor N3150, N3050 and N3000 Product Family.

In these Release Notes, driver interfaces, limitations, errata, closed issues, known issues, platform and driver software best known methods are covered.

This document is intended for OEMs and ODMs that are enabling Win*7 and WES*7 and POSReady7 drivers with the Intel® Atom™ processor x5-E8000, Intel® Pentium® Processor N3700 and Intel® Celeron® Processor N3150, N3050 and N3000 Product Family.

1.2 System Requirements

The following Operating Systems are supported:

- Windows* 7 Operating System (32-bit and 64-bit versions)
- Windows* Embedded Standard 7 Operating System (32-bit and 64-bit versions)
- Windows* Embedded POSReady 7 Operating System (32-bit and 64-bit versions)

1.3 Acronyms and Terminology

Table 1. Acronyms and Terminology

Term	Description
API	Application Programming Interface
ATAPI	ATA Packet Interface
BSP	Board Support Package
CRB	Customer Reference Board
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
HSUART	High Speed Universal Asynchronous Receiver/Transmitter

Term	Description
I2C	Inter-Integrated Circuit
IO	Input Output
IOCTL	Input Output Control
KITL	Kernel Independent Transport Layer
LAN	Local Area Network
MSDN	Microsoft* Developer Network
OS	Operating System
PCI	Peripheral Component Interconnect
SATA	Serial ATA
USB	Universal Serial Bus

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2.0 Release Summary

2.1 Release Details

Driver Version: 1.2.3.0616

Released: March 2016

2.2 Release Contents

The contents of this release include:

- Intel® Processor Win7 IO Drivers 32Bit and 64Bit Driver Installer
- Both "Intel Processor Win7 IO Drivers 32Bit.msi" and "Intel Processor Win7 IO Drivers 64Bit.msi" installers will install the following drivers on your system:
  - Intel® Atom™/Celeron®/Pentium® Processor UART Host Controller
  - Intel® Atom™/Celeron®/Pentium® Processor I2C Controller
  - Intel® Atom™/Celeron®/Pentium® Processor GPIO Controller
  - Intel® Atom™/Celeron®/Pentium® Processor SD/eMMC Controller
  - Intel® Atom™/Celeron®/Pentium® Processor Low Power Subsystem DMA Device
- Intel® Processor Win7 IO Drivers – Software Developer Guide
  - Headers Files for GPIO and I2C
  - Software Developers Manual for Windows 7 IO Drivers
- Intel® Processor Win7 IO Drivers Release Notes & User's Guide
- Intel® Software License Agreement

2.3 Best Known Configurations

Table 2. Best Known Configurations

Hardware Configuration		
Category	**Description**	**Rev/Type/ Source**
CRB	Cherry Hill	Rev F
SOC	Intel® Atom™ processor x5-E8000, Intel® Pentium® Processor N3700 and Intel® Celeron® Processor N3150, N3050 and N3000 Product Family	C0 and D1
Display	HDMI	
Memory	Cherry Hill: 4 GB DDR3 (2x2GB)	
Firmware Configuration		
CRB BIOS	Braswell Cherry Hill CRB BIOS Release Package v93 MR3 (vBIOS 1013)	Refer to BIOS release
KSC	N/A	N/A
Driver/OS Configuration		
Operating System	Windows 7 SP1 Windows Embedded Standard 7 SP1 Windows Embedded POSReady 7 SP1	MSDN
Graphics Driver	38.15.0.1125 (32-bit) 15.38.6.64.4299 (64-bit)	Intel Graphics driver
GPIO Driver	1.2.2.1008	Intel
I^2C Driver	1.2.2.1008	Intel
SPI Driver	N/A	N/A
HS-UART Driver	1.2.3.1010	Intel
SD and eMMC* Driver	1.2.3.1010	Intel
DMA	1.2.3.1010	Intel
Chipset INF	10.1.1.14	Intel
USB 3.0 Driver	4.0.4.51 (32-bit and 64-bit)	Intel

2.4 The Ready Feature

Table 3. Ready Features

Area	Feature	Source	Ready‡
SIO	General SIO feature	Win7 Inbox driver	Yes
USB	General USB 2.0 feature	Win7 Inbox driver	N/A
	General USB 3.0 feature	Intel USB 3.0	Yes
	USB3.0 Boot	Win7 Inbox driver	Yes
SATA	General SATA feature	Win7 Inbox driver	Yes
	General SATA2 feature		N/A
	General SATA3 feature		Yes
PCIe*	General PCIe* feature	Win7 Inbox driver	Yes
Intel® Graphics Driver	General graphics feature	Intel	Yes
High Definition Audio	General HD Audio feature	Win7 Inbox driver	Yes
	HDMI Audio	Integrated in Intel Graphics driver	Yes
Power Management	Power Mgmt S0 and S5	N/A	Yes
	Power Mgmt Sleep S3	Intel	Yes
	Power Mgmt Hibernate S4	Intel	Yes
GPIO Driver[1]	Direction Setting	Intel	Yes
	Multiplexing Setting		Yes
	Level Value Setting		Yes
	Pin Setting Query		Yes
I2C Driver[1]	Standard Mode (100Kbps)	Intel	Yes
	Fast Mode (400Kbps)		Yes
HS-UART Driver[1]	Baud rate support up to 4,000,000	Intel	Yes
	Data size 5, 6, 7, 8-bit		Yes
	Odd, even, none parity		Yes
	1, 1.5, and 2 stop bits		Yes
	Hardware & No flow control & Software flow control		Yes
DMA Feature[1] (I2C, HS-UART)	DMA support for I^2C*, and HS-UART	Intel	Yes
Version 4.5.1 Storage	Version 4.5.1 Storage	Intel	Yes
	Win*7 OS Boot		Yes

Area	Feature	Source	Ready‡
SD2 Driver	SD and SDHC cards	Intel	Yes
	Class 2,4,6,10 and UHS-1		Yes
	1-bit and 4-bit Bus Mode		Yes
	FAT32, NTFS, exFAT File System		Yes
	Advanced Direct Memory Access (ADMA) transfer mode		Yes
	Win*7 OS Boot		Yes

Note: ‡Refer to the next section for the limitations of the GPIO/I²C*/HS-UART/DMA/SD/eMMC* feature.

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3.0 Release Notes

3.1 GPIO Driver

The GPIO Driver interface is exposed by a series of IOCTLs. A separated C header file provides the definition of the IOCTLs and a separated programming guide provides how to program with the IOCTLs.

Driver Binary Package:

- **iaiogpio.inf**
- **iaiogpio.sys**
- **iaiogpio.cat**

Driver Interface Header:

- GPIOPublic.h

Enabled Features:

- Support GPIO multiplexing setting.
- Support GPIO setting query, query multiplexing information of GPIO pin.
- Support GPIO direction setting, configure selected GPIO pin as input or output pin.
- Support GPIO read pin, read pin's level value when GPIO pin is configured as input pin.
- Support GPIO write pin, configure pin level to high or low when it is configured as output pin.

Limitations:

No known limitation

3.2 I²C* Driver

The I²C* Driver interface is exposed by a series of IOCTLs. A separated C header file provides the definition of the IOCTLs and a separated programming guide provides how to program with the IOCTLs.

There are a total of seven I²C controllers on the Intel® Atom™ processor x5-E8000, Intel® Pentium® Processor N3700 and Intel® Celeron® Processor N3150, N3050 and N3000 Product Family which share the same DMA engine. Hence, transferring a big data size will cause one I²C controller to occupy DMA engine for a long duration.

The application can use multiple single transfers or **IOCTL_I2C_EXECUTE_SEQUENCE** interface to transfer big data.

By default, I^2C driver uses DMA to copy data between peripheral and system memory, but can set Windows registry to disable DMA feature and copy data by PIO mode. Refer to the BKM section regarding how set the registry.

Driver Binary Package:

- **iaioi2c.inf**
- **iaioi2c.sys**
- **iaioi2c.cat**

Driver Interface Header:

- **I2CPublic.h**

Enabled Features:

- Support 7-bit address Mode
- Support Standard Mode (100 Kbps)
- Support Fast Mode (400 Kbps)
- Support polling of IO data transfer

Limitations:

The maximum single transfer size is limited to 64 KB. Multiple transfer is required for data size of more than 64 KB.

3.3 HS-UART Driver

HS-UART Driver interface is exposed by standard Windows* Serial Communication interface. Refer to Serial Communications in Win32 in Microsoft* Developer Network (MSDN*) to understand the details.
http://msdn.microsoft.com/en-us/library/ms810467.aspx

Following APIs of serial communication in Win32 are supported in MR1 driver release:

- **SetCommMask**
- **WaitCommEvent**
- **GetCommMask**

Remark: These serial series masks: "`SERIAL_EV_PERR, SERIAL_EV_RX80FULL, SERIAL_EV_EVENT1, SERIAL_EV_EVENT2`" used in the above three functions are not supported. Others are supported.

Intel has no plan to support the following APIs of serial communication in Win32:

- **SetupComm**
- **SetCommBreak**
- **ClearCommBreak**
- **EscapeCommFunction** (no support for parameter set to SETBREAK and CLRBREAK)

Driver Binary Package:

- **iaiouart.inf**
- **iaiouart.sys**
- **iaiouart.cat**

Note: Driver Interface Header: Refer to MSDN* as above link.

Enabled Features:

- Support baud rates as specified in the "N-series Intel® Pentium® Processors and Intel® Celeron® Processors External Design Specification (EDS)" (document#547869), Section 16.3.2.3 Baud Rate Generator.
- Support data size of 5,6,7, and 8-bit
- Support none, odd and even parity
- Support 1, 1.5, and 2 stop bits
- Support "Hardware" and "No" flow control and software flow control
- Supports Serial Device Control Requests (IOCTLs) defined by MSFT for serial controllers in Windows. See Limitations below for the IOCTLs that will be enabled in Gold release.

Limitations:

- HS-UART driver doesn't support DMA transfer with software flow control. When application uses the software flow control, the HS-UART will use PIO mode to copy data between peripheral and system memory.
- Software flow control only supports a maximum baud rate up to 115200. Recommended to use hardware flow control for data transfer for high baud rate.
- When 1.5 stop bits is used, the data size can only be supported up to 5 bits.
- IOCTLs are not supported in driver:

  IOCTL_SERIAL_XOFF_COUNTER

  IOCTL_SERIAL_LSRMST_INSERT

  IOCTL_SERIAL_SET_BREAK_ON

  IOCTL_SERIAL_SET_BREAK_OFF

3.4 LPSS DMA Driver

LPSS DMA Driver is not exposed publicly and only I^2C, HS-UART drivers are able to access the DMA driver interface.

3.5 SD2 Storage Driver

SD2 driver is not exposed publicly and will replace the Windows Inbox SD2 driver to provide SD2 storage capabilities on this Intel SoC platform.

Driver Binary Package:

- **iaiosd.inf**
- **iaiosd.sys**
- **iaiosd.cat**

Driver Interface Header: None

Enabled Features:

- Support SD and SDHC card specification.
- Support SD card class: 2, 4, 6, 10, and UHS-1.
- Support 1-bit and 4-bit bus mode.
- Support FAT32 and exFAT file system.
- Support Advanced Direct Memory Access (ADMA) transfer mode

Limitation:

SD card read & write performance may be 10- 20% lower in Win7/WES7 64 bit due to operating system limitation as the system only sends 64Kb package.

3.6 eMMC Storage Driver

eMMC storage driver is not exposed publicly and will provide eMMC storage capabilities on this Intel SoC platform.

Driver Binary Package:

- **iaiosd.inf**
- **iaiosd.sys**
- **iaiosd.cat**

Driver Interface Header: None

Enabled Features:

- Support eMMC card specification 4.5.1
- Support 8-bit SDR & DDR bus mode.
- Support FAT32 and exFAT file system.
- Support Advanced Direct Memory Access (ADMA) transfer mode.
- Support HS200 mode.

Limitation:

- eMMC card read & write performance may be 10- 20% lower in Win7/WES7 64 bit due to operating system limitation as the system only sends 64Kb package.
- Driver don't support 1-bit and 4-bit bus modes

3.7 SD and eMMC Boot Driver

SD and eMMC boot driver is not exposed publicly and it will enable Windows 7 OS to be installed into these storage devices enabled on this Intel SoC platform.

Driver Binary Package:

- **iaiosd.inf**
- **iaiosd.sys**
- **iaiosd.cat**

Driver Interface Header: None

Enabled Features:

Supports Windows 7 32 and 64-bit OS installation and boot with S3 and S4 enabled.

Limitation:

No Known Limitations.

3.8 Errata, Closed Issues, Known Issues

3.8.1 Errata

Table 4. Errata

Issue #	Description	Impact	Recommendation
4634937	HS-UART COM number increases every time after uninstall/reinstall of UART driver	For those applications using COM ports of HSUART, user need to enable changing input parameter of COM number	Change the HS-UART COM ports in the application whenever the UART driver is reinstalled.
4635034	System unable to load into Windows after wake up from hibernate by hitting USBkeyboard and mouse when XHCI mode in BIOS is set to 'Auto' or 'Smart Auto'	User failed to resume the system back from hibernate when XHCI mode is set to "Auto" or smart Auto	Change XHCI mode to "Enable".
5221264	[CHH][WES7] UART data mismatch when running the test with None and Software flow control	Customer cannot use HS-UART at certain baud rate reliably	Use hardware flow control. Max baud rate for software and none flow control is 115200.

3.8.2 Closed Issues

Table 5. Closed Issues

Issue #	Description	Resolution
N/A		

3.8.3 Known Issues

Table 6. Known Issues

Issue #	Description	Impact	Recommendation
5221392	[CHH][WIN7] USB3.0 Read/Write not up to expectation.	Very fast USB3.0 device will notice drop in performance.	Still can be used and within USB3.0 range.
1207100978	[CHH][WES7] BSOD when booting SUT to OS on USB storage device.	BSOD when booting WES7 with certain USB installation media.	Issue under investigation, there is no planned workaround at this time.

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